

Advances in grayshade performance of active matrix electroluminescent (AMEL) microdisplays

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ABSTRACT

There exist many applications in military and commercial fields where rugged, lightweight microdisplays are required for helmet mounted and viewfinder display systems. Such applications typically involve the display of high resolution symbology but increasingly also include the display of full motion video. Examples of these kinds of image sources include thermal imaging and weapon sighting.

Active matrix electroluminescent (AMEL) microdisplay technology developed at Planar has uniquely satisfied the demanding environmental and power requirements of military and commercial helmet mounted display and viewfinder systems. Recent advances have extended the use of AMEL microdisplays to applications requiring the display of high grayscale content, while significantly reducing the size, cost, and power of the system electronics required to drive the display.

This capability has been enabled through the development of an analog addressing architecture. This paper provides a background of the analog architecture and the advantages gained by using this approach. Specifications and interface requirements are discussed for a monochrome 640x512 display developed using this architecture.

Keywords: AMEL, microdisplay, head-mounted display, electroluminescence

1. BACKGROUND

Since the initial introduction of active matrix electroluminescent (AMEL) microdisplays into the marketplace over four years ago, continued developments have focused on improving the grayshade performance. Incremental improvements have been made resulting in performance that is sufficient for displaying imagery with high grayshade content¹. This has enabled the use of AMEL microdisplays in applications such as thermal imaging and night vision systems.

The objective of the work described in this paper was to develop a new architecture for easing the interface of AMEL microdisplays to today's common video sources while providing a further improvement in grayshade performance. This was made possible by changing the display architecture from that of a digitally addressed pixel array to an analog array.

2. WHY ANALOG?

Most of today's common image sources output data in a 'grayscale parallel' or 'color parallel' format where all grayscale or color information is output to the video interface one pixel at a time (Fig. 1). This is true for the ubiquitous 15-pin RGB analog output found on most personal computers as well as for video standards such as RS-170, CCIR, NTSC, and PAL. This continues to be the case even for the new digital PC interface standards starting to emerge, such as digital flat panel (DFP) and digital video interface (DVI).

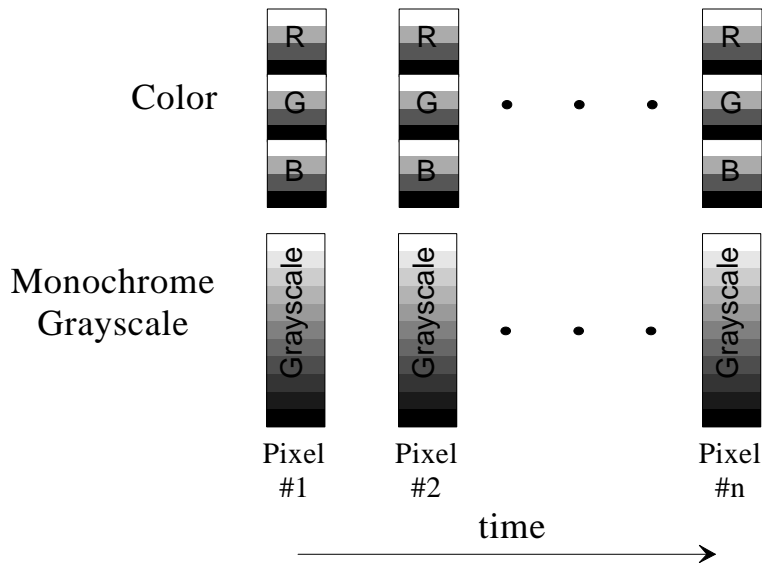


Figure 1. Grayscale parallel / color parallel interface

Many microdisplay technologies incorporate an active matrix pixel array that requires update in a bit sequential or color sequential format (Fig. 2). In the case of the previously developed digital AMEL technology, the display must be fully addressed multiple times within a frame to achieve grayscale. This is because the appearance of grayscale is achieved through modulating the ‘on’ time of pixels via a binary weighting scheme. Fig. 3 depicts this scheme for a 5-bit, or 32 graylevel scheme. A variation on this approach is commonly used to generate over 100 graylevels¹.

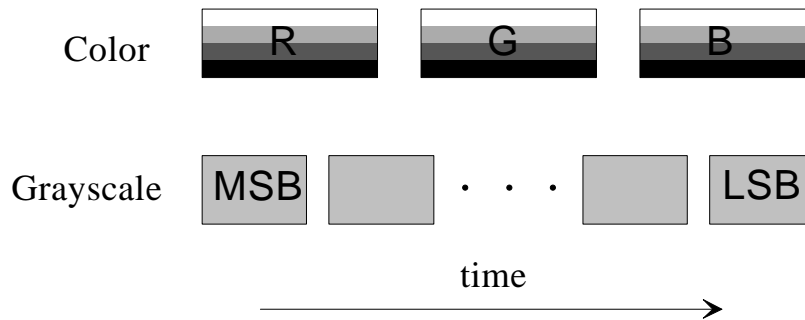


Figure 2. Timing required for bit-sequential or color sequential addressing

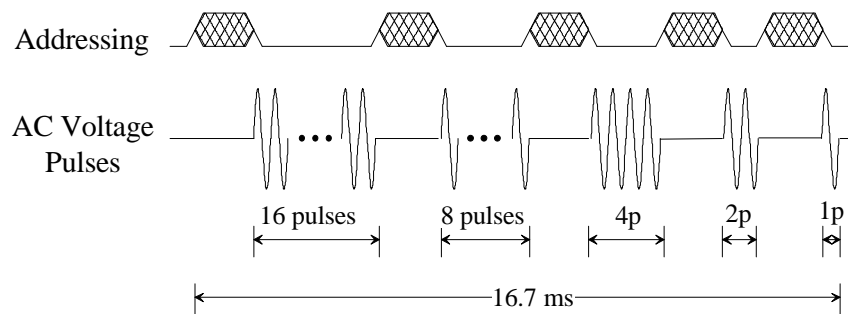


Figure 3. Grayscale implementation using the digital AMEL pixel architecture

The primary drawback of the bit sequential and color sequential addressing schemes is that a rather complicated digital processing function must be performed by the interface electronics to convert from the format of the commonly available

image sources to the bit sequential or color sequential formats required by the microdisplay. For every frame, the incoming data has to be accumulated in a frame memory device, and then output to the display in the proper format during the next frame. As shown in Fig. 4, this requires frame memory and complex control logic devices. This in turn requires additional space for electrical components and adds a significant amount of power. A further drawback of this approach is that there is a one-frame lag between the display update and the incoming image data.

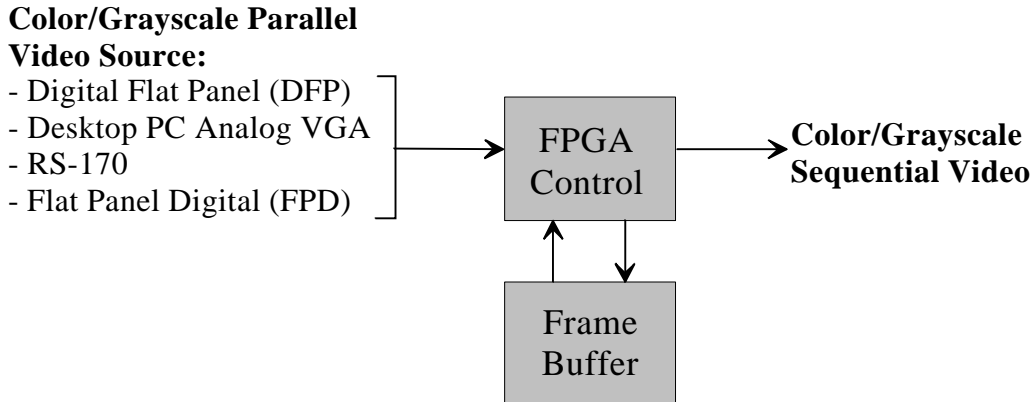


Figure 4. Block diagram of data flow required for conversion of common image stream formats to bit sequential or color sequential formats.

In some cases it may be possible to alter the system architecture so that data is output from the sensor or image generator in this format. However, it is a very unusual case where the system engineer has this degree of freedom. Generally, the display sub-system must be altered to make do with the format provided by the other components. Almost invariably, this means interfacing to a pixel parallel format such as that shown in Fig. 1.

By going to an analog ‘native’ architecture, data can be written directly to the microdisplay in a grayscale or color parallel format. No complex frame buffering and image processing steps are needed. Data is written to the pixel cells as it arrives from the interface. Therefore, the frame buffer and data control blocks are eliminated. This results in significantly simpler interface electronics, which in turn reduces system cost, power and size.

3. ANALOG PIXEL ARCHITECTURE

The digital and analog pixel cell diagrams are shown in Fig. 5. As reported previously^{2,3,4}, in the digital cell the source of the DMOS transistor is typically connected to ground. For the analog case, the source of the DMOS is connected to a ramp line. This line linearly increases from low to high throughout the field. Once the ramp voltage exceeds the voltage on gate of the pixel cell (minus the DMOS threshold voltage), the DMOS turns off and the pixel stops emitting light. By using this ramp technique, the DMOS acts as a comparator. The key advantage of this approach is that it is not necessary to modulate the DMOS near its threshold for analog grayscale control.

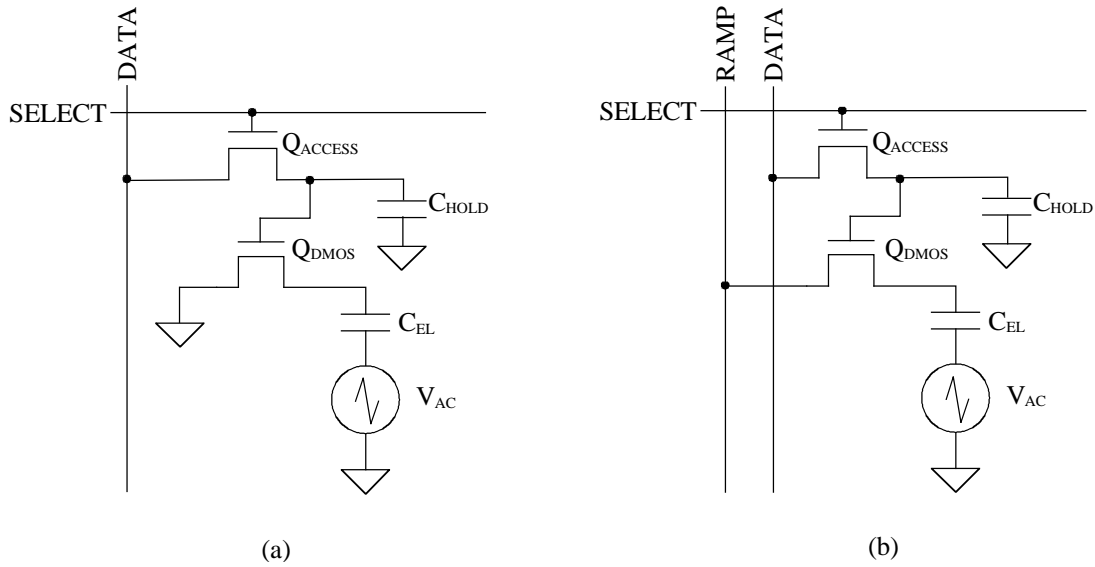


Figure 5. Pixel circuit designs: (a) digital cell with DMOS source grounded and (b) analog cell with DMOS source connected to RAMP line. In the analog case, the DMOS works as a comparator; when the RAMP value exceeds the voltage on the gate of the DMOS (minus the DMOS threshold voltage), the transistor turns off and there is no light emission.

In Fig. 6 the expected light output using the analog system is shown for different voltage levels stored on the hold node. Every AC cycle results in two light pulses: one during the positive half cycle and one during the negative half cycle. For a low value of V_{HOLD} , the RAMP value quickly achieves a value greater than that stored on the hold node, and little or no light is emitted. For higher values of hold node voltage, the DMOS transistor stays on longer and therefore more light is emitted. The eye averages the number of light pulses into a perceived level of luminance (grayscale).

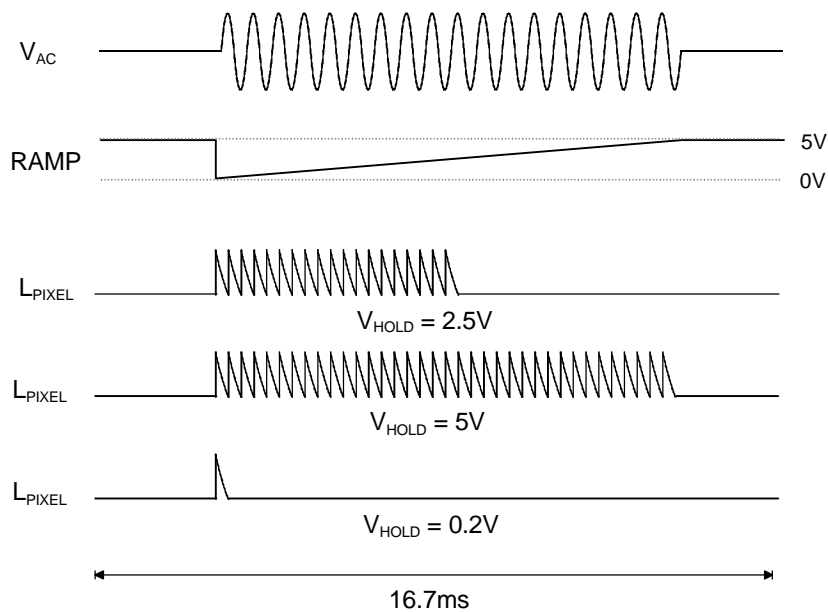


Figure 6. Light output as a function of different voltages stored in the hold element.

Fig. 6 can be interpreted as a first order approximation of the light output. This depiction suggests that grayscale resolution is limited by the number of AC pulses applied during the frame, since the light pulses are quantized by the AC pulses. Experimental results have shown that near the region of pixel turn-off (threshold), there is actually a range where the pixel is only partially turned off, and is modulating the voltage on the DMOS drain. This in turn results in a modulation of the pixel luminance in this region (Fig. 7). Therefore, the grayscale response makes very soft transitions through the levels.

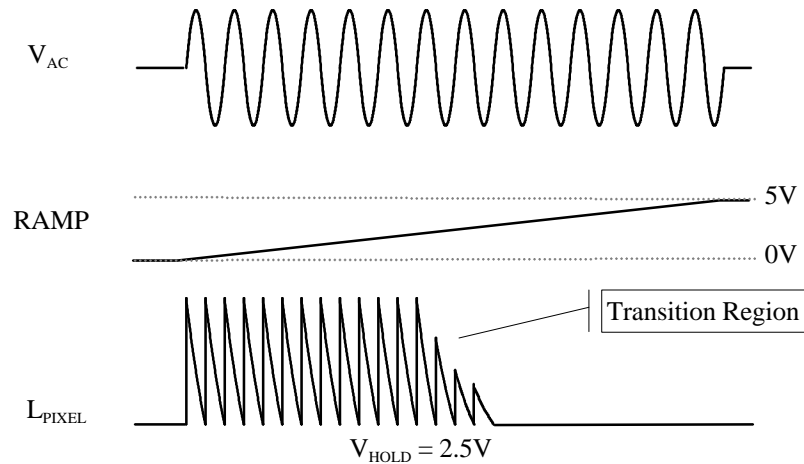


Figure 7. Magnified view of region where ramp transitions from below V_{HOLD} value to above V_{HOLD} .

4. INTERFACE ELECTRONICS

An example block diagram for interface electronics used in conjunction with RS-170 or 15-pin Analog VGA input is shown in Figure 8. The primary components required are as follows:

- 1) AC Inverter – External source for AC pulses required for light emission from EL films
- 2) Sync Separator – Extracts horizontal sync (HS) and vertical sync (VS) from composite video. Also generates a signal to tell the display whether the odd or even field is being presented.
- 3) Clock Generator – Re-generates a pixel clock from the horizontal sync
- 4) Ramp – Linearly increasing ramp signal for pixel comparators (runs at field rate)
- 5) Video Amplifiers – Amplifies signal from 1V or 0.7V to 5V level required by display
- 6) Power Supplies – 5V, 7.5V, and -2V required for on-chip timing and control circuits

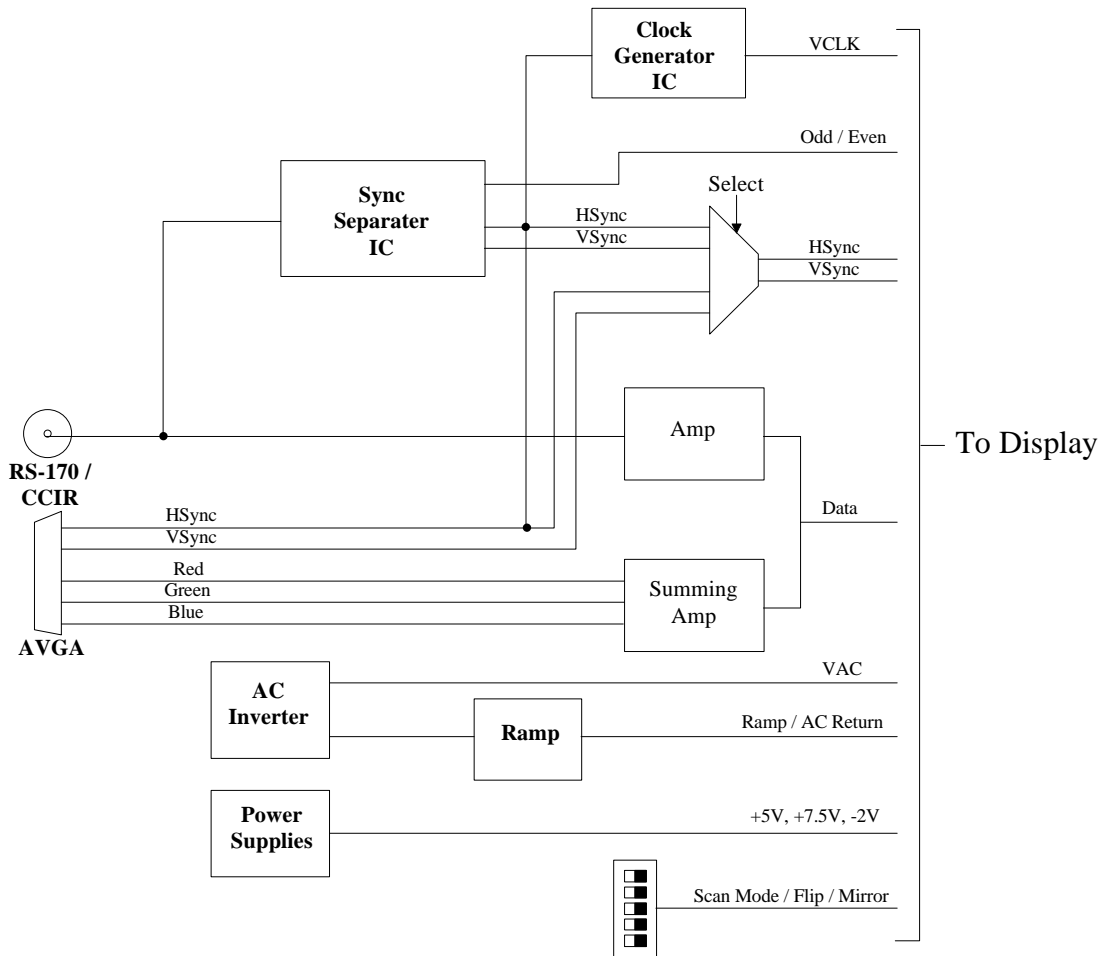


Figure 8. Block diagram example of RS-170 / analog VGA interface to a monochrome analog AMEL display.

5. 640 X 512 DISPLAY SPECIFICATION

The first display format developed using this analog address approach is a monochrome amber 640x512 display incorporating a 24 μ m pixel pitch, resulting in a 19.7mm (0.77-in.) diagonal.

A key objective in the design of this format was to simplify the interface to common image sources. In addition to providing for direct analog input, a simple vertical sync (VS), horizontal sync (HS) and video clock timing format was used. This was accomplished with the integration of a timing generation circuit on the same IC as the microdisplay. All internal timing required for operation of the data de-multiplexing circuit, row select circuits, and other on-chip control circuits is provided by this function block.

Additional functionality was provided for interfacing to interlaced video sources such as RS-170 and CCIR. Multiple interlace addressing modes are supported so that the user or system integrator can select one to minimize de-interlacing artifacts for the target application. Table 2 lists these interlacing modes.

Table 2. Scan modes supported by the monochrome analog AMEL 640x512 microdisplay

Scan Mode	Description
Progressive	A/B/C/D/E/...
Progressive Double	AB/CD/EF/GH/...
Interlace Double	Odd Frame: AB/CD/EF/GH/ Even Frame: A/BC/DE/FG/HI/...
Interlace with Blanking	Odd Frame: A/B0/C/D0/E/F0/G/ Even Frame: A0/B/C0/D/E0/F/G0/H/...
Interlace without Blanking	Odd Frame: A/C/E/G/ Even Frame: B/D/F/H/...

A,B,C,... refers to first row, second row, third row, etc. addressed on display.

A0,B0,C0,... refers to blanked rows (all pixels in row addressed to 'off')

In addition to these scan modes, support for image flip and mirror was designed into the display. These functions accommodate most kinds of display and optical orientations found in HMD and viewfinder systems. The flip function is accomplished by reversing direction of the vertical scan. Likewise, the mirror function is accomplished by reversing direction of the horizontal data scan.

A summary of the specifications for this display design are shown in Table 3.

Table 3. Preliminary specification summary for the monochrome 640 x 512 AMEL display utilizing the analog architecture

Specification	Value
Pixel Format	640 (H) by 512 (V)
Pixel Pitch	24 μ m x 24 μ m (0.945 x 0.945 in)
Viewable Area	15.4 x 12.3 mm (0.605 x 0.484 in)
External Package (LxW)	25.65 x 23.46 mm (1.01 x 0.923 in)
Thickness	3.73 mm (0.147 in)
Weight	< 3g
Pixel Fill Factor	84%
Data Refresh	25 to 80 Hz
EL Excitation Amplitude	140 to 200V
EL Excitation Frequency	0.5 to 10 KHz
Luminance	
High Luminance Mode	500fL
Standard Luminance Mode	50fL
Power Consumption	
High Luminance Mode	2.0W
Standard Luminance Mode	0.4W
Contrast Ratio	> 100:1
Operating Temperature	-40 to 75C
Storage Temperature	-55 to 85C

6. FUTURE DIRECTION

The next step in development of the analog AMEL technology will focus on full color formats. The approach used for color incorporates a broadband emitting thin film stack⁵. The color pixel is broken down into separate red, green, and blue sub-pixels, each addressed independently. The electrodes are arranged in long and narrow stripes to form a square color pixel. The individual colors are achieved by filtering the light using color filter materials patterned over the sub-pixels. Formats planned using this approach include a color 640x512 array using 24 μ m pitch color pixels, resulting in a 19.7mm (0.77-in) diagonal. Also planned is a color 800x600 array in approximately 22.9mm (0.9-in) diagonal.

By using the patterned color filter approach, all the advantages of the analog AMEL architecture are leveraged for the color format as well. As with the monochrome format described above, there is no need for frame buffering and complex control logic. Additionally, a significant improvement in the number of colors is expected.

7. ACKNOWLEDGMENTS

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8. REFERENCES

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